Amendments to the Specification:

In paragraph [0001]:

The invention relates to a phase locked loop for controlling an optical recording device, and more particularly, to a phase locked loop having a phase-shift detector and a phase-controllable frequency divider for ~~controllingan~~ controlling an optical recording device.

In paragraph [0002]:

In a conventional recordable optical ~~disk,such~~ disk, such as a DVD-R/RW disk or a DVD+R/RW disk, a wobble signal is used as a reference to generate a write clock for recording data on an optical disk. A phase locked loop (PLL) is commonly applied for generating the required write clock with reference to the wobble signal. Please refer to Fig.1, which is a diagram of a related art PLL 10. As shown in Fig.1, the related art PLL 10 generates an output clock in response to a wobble signal extracted from the wobble tracks on a recordable optical disk. The output clock is used to be the reference for the recording bit clock. The PLL 10 includes a phase detector (PD) 20, a charge pump 30, a loop filter 40, a voltage-controlled oscillator (VCO) 50, and a frequency divider 60. The PD 20 is used to output a phase error signal to the charge pump 30 by detecting the phase difference between the wobble signal and a divided signal generated from the frequency divider 60. The charge pump 30 is used to generate a voltage based on the phase error signal from the PD 20. After the loop filter 40 receives the voltage outputted from the charge pump 30, the loop filter ~~40outputs~~ 40 outputs a control voltage to control the following VCO 50. The VCO 50 receives the control voltage outputted from the loop filter 40, and generates the output clock according to the control voltage. Generally, the frequency of the output clock signal is higher than that of the wobble signal, so that the frequency divider 60 is required for dividing the frequency of the output clock outputted

from the VCO 50 to generate the frequency-divided signal delivered to the PD 20.

In paragraph [0003]:

However, the related art PLL 10 sometimes cannot make the phase of the output clock in synchronization with the phase of the wobble signal due to the limitation of the PD 20, which is called the phase shift phenomenon. Please refer to Fig.2, which ~~illustratesthe~~ <u>illustrates the</u> phase shift phenomenon of the related art. The horizontal axis represents the phase ~~difference θe~~ <u>difference θe</u> between the wobble signal and the frequency-divided signal inputted into the PD 20, and the vertical axis stands for the phase ~~error μ_d~~ <u>error μ_d</u> outputted from the PD 20. In addition, the symbol $\triangle W_d$ is the detection range of the PD 20. As shown in Fig.2, it can be easily seen that the phase ~~difference θe~~ <u>difference θe</u> is not necessarily equal to zero when the phase ~~error μ_d~~ <u>error μ_d</u> equals zero. If the phase ~~difference θe~~ <u>difference θe</u> is within the detection range $\triangle W_d$ of PD 20, such as the point B shown in Fig.2, the PLL 10 tracks and reduces the phase ~~difference θe~~ <u>difference θe</u> to zero (the point A shown in Fig.2). However, if the phase ~~difference θe~~ <u>difference θe</u> is outside the detection range $\triangle W_d$ of the PD 20, such as the point C shown in Fig.2, the outputted phase ~~error μ_d~~ <u>error μ_d</u> makes the PLL 10 lock the phase to ~~thenearest~~ <u>the nearest</u> zero-crossing point (the point D shown in Fig.2), rather than the desired one (the point A shown in Fig.2). Therefore, ~~theappearance~~ <u>the appearance</u> of the phase shift phenomenon makes the PLL 10 malfunction.

In paragraph [0025]:

Fig.15 is a block diagram of a PLL system according to a seventh embodiment of ~~thepresent~~ <u>the present</u> invention.

In paragraph [0029]:

Please refer to Fig.5 in conjunction with Fig.4. Fig.5 is a flow chart illustrating the operation of tuning the count value CNT utilized by the phase-controllable frequency divider 160 shown in Fig.4. As mentioned above, the phase-controllable frequency divider 160 is connected to the VCO 150 for receiving the output clock. In this embodiment, the counter 162 within the phase-controllable frequency divider 160 is trigged by each cycle of the output clock, and then the phase-controllable frequency divider 160 controls the phase of the frequency-divided signal according to the count value CNT of the counter 162, in which the threshold value N is the dividing ratio of the phase-controllable frequency divider 160. In other words, if the frequency of the output clock is equal to F, the frequency of the frequency-divided signal equals (F÷N). As described before, the phase shift phenomenon in the related art affects the PLL system 110 to lock to the desired phase for the output clock. To solve the problem of phase shift phenomenon, the phase-shift detector 170 measures the actual phase shift deviated from the desired phase, and outputs the phase-adjusting signal to the phase-controllable frequency divider 160 according to the detected phase shift. In this embodiment, an offset value is transmitted to the phase-controllable frequency divider 160 through the phase-adjusting signal. The operation of setting the count value CNT is detailed as follows. When the counter 162 within the phase-controllable frequency divider 160 is triggered by a rising edge or a falling edge of a cycle of the output clock, the count value CNT is required being updated (step 182). Then, the existence of the offset value is checked (step 183). If the phase-shift detector 170 detects a phase shift affecting the output clock, the offset value is delivered to the phase-controllable frequency divider 160 and the count value CNT is updated by a new value equaling CNT+offset+1 (step 184). On the contrary, if the phase-shift detector 170 detects no phase shift affecting the output clock, the count value CNT is updated by a new value equaling CNT+1 (step 185). Then, if the newly updated count value CNT is equal to or larger than the threshold value ~~N,.~~ N, the count value CNT is further updated by a new value equaling CNT-N (step 187).

In paragraph [0030]:

Please refer to Fig.6 in conjunction ~~withFigs.4~~ with Figs.4 and 5. Fig.6 is a timing diagram illustrating the operations of the phase-shift detector 170 and the phase-controllable frequency divider 160 shown in Fig.4, in which the dividing ratio N is equal to 8 and the waveform of the frequency-divided signal is equal to the logic value of that the count value CNT≧4. As shown in Fig. 6(a), if the phase-shift detector 170 is disabled, the count value CNT is counted normally, and the rising edge of the frequency-divided signal S is aligned to when the count value CNT is equal to 4. However, when the phase-shift detector 170 is activated to detect the phase shift for generating the offset value, the count value CNT is tuned to adjust the phase of the frequency-divided signal S. As shown in Fig. 6(b), ~~It is~~ it is easily seen that the phase of the frequency-divided signal S is controlled to lead the phase of the frequency-divided signal S of Fig. 6(a) when the offset value is set to a positive value (e.g. +1 or +2). As shown in Fig. 6(c), the phase of the frequency-divided signal S is controlled to lag the phase of the frequency-divided signal of Fig. 6(a) when the offset value is set to a negative value (e.g. -1 or -2). As shown in Figs.5 and 6, when the phase-shift detector 170 does not transfer any phase-shift signal to the phase-controllable frequency divider 160, the offset value is 0 and the counter 162 sequentially counts the cycles of the output clock for generating the frequency-divided signal. But if the phase-shift detector 170 transfers the phase-shift signal to the phase-controllable frequency divider 160, the offset value is +1, +2, -1,or -2, and the count value CNT is changed according to the inputted offset value, so that the phase of the frequency-divided signal is therefore shifted according to the phase shift detected by the phase-shift detector 170.

In paragraph [0031]:

In addition to the method shown in Fig.5, it can also adjust the phase of the frequency-divided signal ~~bytemporarily~~ by temporarily altering the dividing ratio of the counter 162. The phase of the frequency-divided signal is changed if the dividing ratio of the counter 162 varies. In other words, one period of the frequency-divided signal outputted from the phase-controllable frequency divider 160 is increased or decreased according to the phase-adjusting signal from the phase-shift detector 170. For example, the counter 162 can be a counter that increases normally and is normalized to zero when the value of the counter is equal to the adjustable threshold value ~~N,in~~ N, in which the threshold value N is adjusted according to the phase-adjusting signal from the phase-shift detector 170.

In paragraph [0032]:

Please refer to Fig.7, which is a diagram illustrating the operation of adjusting the phase of the output clock locked in a wrong point to reach a correct point according to the present invention. The horizontal axis represents the phase difference between the wobble signal and the frequency-divided signal inputted into the PD 120, and the vertical axis stands for the phase error outputted from the PD 120. In Fig.7, ~~thecircle~~ the circle symbol "○" is used to stand for the phase of the frequency-divided signal outputted from the phase-controllable frequency divider 160, and the triangle symbol "△" is used to stand for the phase of the output clock. As shown in Fig.7(a), a situation is shown that ~~he~~ the output clock is locked to an incorrect phase at the zero-crossing point pt2, rather than the correct phase at the zero-crossing point pt1. Initially, in Fig. 7(a), the phase of the frequency-divided signal is equal to the phase of the output clock, so that the circle symbol ~~"○"and~~ "○" and the triangle symbol "△" ~~is~~ are placed at the same point pt2.

In paragraph [0033]:

Firstly, as shown in Fig 7(b), the phase-controllable frequency divider 160 adjusts the phase of the frequency-divided signal by a phase increment θ_{p1} to increase the phase difference between the wobble signal and the frequency-divided signal according to the phase-adjusting signal outputted from the phase-shift detector 170. After the phase of the frequency-divided signal is adjusted, the phase of the frequency-divided signal (the circle symbol "○") is moved with the distance ~~of θ_{p1}~~ of θ_{p1} away from the point pt2, while the phase of the output clock (the triangle symbol "△") is still at the point ~~pt2.Then~~ pt2. Then, as shown in Fig 7(c), the PLL system 110 works to ~~minimizethe~~ minimize the phase error ~~signalof~~ signal of the phase detector (PD) 120. That is, the PLL system 110 lags the phase of the output clock (the triangle symbol "△") by the phase ~~increment θ_{p2}~~ increment θ_{p2} to make the phase of the frequency-divided signal (~~thecircle~~ the circle symbol "○") back into the nearest zero crossing point, i.e. the point pt2. As a result, the overall phase shift of the output clock is reduced with a mount ~~of θ_{p1}.Secondly~~ of θ_{p1}. Secondly, as shown in Fig 7(d), the phase-controllable frequency divider 160 further adjusts the phase of the frequency-divided signal by a phase increment θ_{p2} to increase the phase difference between the wobble signal and the frequency-divided signal according to the phase-adjusting signal outputted from the phase-shift detector 170. After the phase of the frequency-divided signal is adjusted, the phase of the frequency-divided signal is moved with the distance ~~of θ_{p2}~~ of θ_{p2} away from the point pt2, At this time, the accumulated phase adjust is equal ~~to θ_{p1}~~ to $\theta_{p1} + \theta_{p2}$, which is also the difference between the phase of the frequency-divided signal and the output ~~clock.Then~~ clock. Then, as shown in Fig 7(e), the PLL system 110 works again to ~~minimizethe~~ minimize the phase error signal of the phase detector (PD) 120. That is, the PLL system 110 lags the phase of the output clock by the phase ~~increment θ_{p2}~~ increment θ_{p2} to make the phase of the frequency-divided signal back into the point pt2. As a result, the overall phase shift of the

output clock is further reduced with an additional mount ~~of θ_{p2}. Finally~~ of θ_{p2}. Finally, as shown in Fig 7(f), the phase-controllable frequency divider 160 further adjusts the phase of the frequency-divided signal by a phase increment θ_{p3} to increase the phase difference between the wobble signal and the frequency-divided signal according to the phase-adjusting signal outputted from the phase-shift detector 170. After the phase of the frequency-divided signal is adjusted, the phase of the frequency-divided signal is moved with the distance ~~of θ_{p3}~~ of θ_{p3} away from the point pt2, At this time, the accumulated phase adjust is equal ~~to θ_{p1}~~ to $\theta_{p1} + \theta_{p2} + \theta_{p3}$, which is also the difference between the phase of the frequency-divided signal and the output clock. Then, as shown in Fig 7(g), the PLL system 110 works again to ~~minimizethe~~ minimize the phase error signal of the phase detector (PD) 120. That is, the PLL system 110 lags the phase of the output clock by the phase ~~increment θ_{p3}~~ increment θ_{p3} to make the phase of the frequency-divided signal back into the point pt2. As a result, the overall phase shift of the output clock is further reduced with an additional mount ~~of θ_{p3}.~~ of θ_{p3}. As mentioned above, the offset values computed by the phase-shift detector 170 are capable of gradually tuning the phase of the output clock to eliminate the related art phase shift phenomenon imposed upon the output clock.

In paragraph [0034]:

When the phase adjusting operation ~~responses~~ responds to the output of VCO 150, the variation of output clock is very smooth due to the loop filter 140. Please note that the phase ~~adjustments θ_{p1},~~ adjustments θ_{p1}, θ_{p2}, θ_{p3} are suggested not ~~exceeding a~~ exceeding a half of the detection range ~~$\triangle W_d$ to~~ $\triangle W_d$ to make the control of the phase adjusting as simple as possible. If one of the phase adjustments θ_p is greater than half of the detection range $\triangle W_d$, the PLL system 110 locks the phase of the output clock to another phase further deviated from the desired one, which means the control of the phase

adjusting is complex. Besides, no matter how large the amount of unwanted phase shift is, the present invention is capable of adjusting the phase shift by a plurality of phase adjustments. As mentioned above, the phase ~~adjustment θ_p~~ <u>adjustment θ_p</u> can be smaller than half of the detection range $\triangle W_d$. For example, if the detection range $\triangle W_d$ is 8T and the initial amount of detected phase shift is 48T, the selected phase increment θ_p can be defined as 2T and it only needs 24 (48T/2T) times of phase adjustments to compensate the phase shift imposed upon the output clock. Moreover, it needs to keep the time between two adjacent phase adjustments long enough to make the PLL system 110 minimize the phase error caused by the phase adjustment.

In paragraph [0036]:

Please refer to Fig.8, which is a block diagram of a PLL system 210 according to a first embodiment of the present invention. The PLL system 210 comprises a first PD 220, a charge pump 230, a loop filter 240, a VCO 250, a phase-controllable frequency divider 260, and a phase-shift detector 270. In this embodiment, the phase-shift detector comprises a second PD 280 and a frequency divider 290. The frequency divider 290 divides the frequency of the output clock, and sends the divided clock into the second PD 280. Therefore, as shown in Fig.8, the second PD 280 is capable of detecting the phase difference between the divided clock of the frequency divider 290 ~~andthe~~ <u>and the</u> wobble signal to estimate the phase shift imposed upon the output clock. Please note that the phase-controllable frequency divider 260 divides the frequency of the output clock by N, but the frequency divider 290 is used to divide the frequency of the output clock by K, where K>N, to make the detection range of the second PD 280 larger than the one of the first PD ~~220.For~~ <u>220. For</u> example, assume that k is set to 32, and N is set to 8. Concerning the DVD+R/RW application that the period of the wobble signal is 32T, if the phase shift is larger than 4T but lower than 16T, the first PD 220 is unable to detect the

phase shift, but the second PD 280 can detect this phase shift. Therefore, the phase shift detector 270 of this embodiment is capable of generating the phase-adjusting signals to the phase-controllable frequency divider 260 according to the detected phase shift.

In paragraph [0037]:

Similarly, please refer to Fig.9, which is a block diagram of a PLL system 310 according to a second embodiment of the present invention. The PLL system 310 also comprises a first PD 320, a charge pump 330, a loop filter 340, a VCO 350, a phase-controllable frequency divider 360, and a phase-shift detector ~~370.In~~ 370. In addition, the phase-shift detector 370 comprises a second PD 380, a first divider 390, and a second divider 400. The only difference between the first embodiment and this second embodiment is ~~thesecond~~ the second divider 400, which divides the wobble signal so that the detection range is capable of being larger than that in the first embodiment.

In paragraph [0038]:

Please refer to Fig.10, which is a block diagram of a PLL system 410 according to a third embodiment of the present invention. The PLL system 410 also comprises a first PD 420, a charge pump 430, a loop filter 440, a VCO 450, a phase-controllable frequency divider 460, and a phase-shift detector 470. The phase-shift detector 470 comprises a second PD 480. Here, the output clock is outputted into ~~the~~ a recorder 490 as the reference for the recording bit clock. In this embodiment, the recorder 490 outputs a recording sync ~~signal , which~~ signal, which is synchronous to the recording ~~data,to~~ data, to the second PD 480 as a reference. As shown in Fig.10, the second PD 480 generates phase-adjusting signals according to the phase difference between the wobble signal and the recording sync signal from the recorder 490. For example, in the application of DVD+R/RW or DVD-RW, each 1456 recording bits plus 32 bits frame sync for total 1488

recording bits are constructed into a frame. In this case, the recording sync signal can be the frame sync signal that is synchronous to the frame sync of the recording data. In addition, the phase-shift detector 470 can further comprise an optional frequency divider 500 shown in Fig.10. This optional frequency divider 500 divides the frequency of the wobble signal. Thus, the detection range of the second PD 480 is enlarged.

In paragraph [0039]:

In addition to the wobble signal, the wobble tracks on a recordable optical disk also comprises some address information corresponding to a location on the recordable optical disk, which is called the physical address and is used to find the position where the recording data to be recorded, such as the ADIP (Address-in-Pregroove) information for the DVD+R/RW and the LPP (Land Pre-pits) information for the ~~DVD-R/RW~~ <u>DVD-R/RW.</u> The information related to the physical address can also be used as the reference for the phase-shift detector. Please refer to Fig.11, which is a block diagram of a PLL system 510 according to a fourth embodiment of the present invention. This embodiment is quite similar to the first embodiment shown in Fig.10. However, the phase-shift detector 570 comprises an ADIP unit sync detector 590. Apparently, this embodiment is applied to the application of DVD+R/RW. The ADIP unit sync detector 590 can generate an ADIP unit sync signal used for indicating the phase change of the first wobble within an ADIP unit (8 wobbles). According to the DVD+R/RW specification, the period of one ADIP unit corresponds to 93 wobbles. As shown in Fig.11, the phase-shift detector 570 uses the ADIP unit sync signal ~~andthe~~ <u>and the</u> divided output clock generated from the frequency divider 600 to generate the phase-adjusting signal.

In paragraph [0040]:

Please refer to Fig.12, which is a block diagram of a PLL system 610 according to a

fifth embodiment of the present invention. This embodiment is similar to the third embodiment shown in Fig.12. It is the same that the recording sync signal is utilized as a reference of the second PD 680. The difference is to utilize the ADIP unit sync signal as another reference of the second PD 680. Therefore, the phase-shift detector 670 generates the phase-adjusting signal according to the phase difference between the recording sync signal and the ADIP unit sync signal. According to the DVD+R/RW specification, an ideal phase difference between the begin of the odd frame of recording data and the begin of an ADIP unit is defined to be 16 wobbles, and the actual phase difference between them can be obtained by detecting the actual phase difference between the recording sync signal and the ADIP unit sync ~~signal.If~~ signal. If the actual phase difference is different from the ideal one, the phase shift imposed upon the output clock can be correctly estimated.

In paragraph [0042]:

As mentioned above, the phase-shift detector generates phase-adjusting signals according to the phase difference between two reference signals (for example, a wobble signal and an ADIP unit sync signal). In fact, it can also generate phase-adjusting signals according to the position difference between the ideal position ~~andtheactual~~ and the actual position of recording data. As shown in Fig.3, the data length of the recorded data is too long or too short due to the phase shift phenomenon, and it can detect the position deviation estimate the phase shift. Please refer to Fig.13, which is a block diagram of a PLL system 710 according to a sixth embodiment of the present invention. In this embodiment, the phase-shift detector 770 comprises a position difference detector 780 instead of the phase detector utilized in above-mentioned embodiments. The output clock is inputted into the encoder 800 for driving the encoder 800 for encoding and recording the recording data, in ~~whicha~~ which a recording data address corresponding to the recording data can be provided. When the recording data are being recorded onto a

recordable optical disk, the encoder 800 outputs the corresponding recording data address to the position difference detector 780.

In paragraph [0043]:

In this embodiment, the phase-shift detector 770 further comprises a physical address detector 790 for detecting the physical address on the recordable optical disk (e.g. a DVD+R/RW disk or a DVD-R/RW disk) through a well-known push-pull signal detected from the recordable optical disk. The phase-shift detector 770 generates the phase-adjusting signal according to the position difference between the recording data address and the detected physical address. In this embodiment, the phase-shift detector 770 generates the phase-adjusting signal according to if the difference between the recording data address and the detected physical address is different from an ideal one.

In paragraph [0047]:

Please refer to Fig.16, which is a diagram illustrating the operation of the PLL system 810 shown in Fig.15. Similar to Fig.16, the track $TRACK_1$ shows the ideal positions of a plurality of data blocks $DATA_5$, $DATA_6$, $DATA_7$, ~~$DATA_8$;~~ $DATA_8$. It is obvious that each of the data blocks $DATA_5$, $DATA_6$, $DATA_7$, $DATA_8$ has an identical data length.

In paragraph [0048]:

Concerning a data block $DATA_5$' having been recorded onto a recordable optical disk ~~at~~ during a previous recording operation and having a data length longer than a desired data length defined by the data block ~~$DATA_5$. When~~ $DATA_5$, when the logical address detector 900 receives the reproduced EFM signal generated from the data block $DATA_5$'

recorded on the recordable disk, the logical address detector 900 detects a logical address of the data block $DATA_5$'. In addition, the physical address is detected by the physical address detector 890 through a well-known push-pull signal read from the recordable optical disk. Then, the position difference detector 880 detects an initial position difference d_{ini}, of the recorded data block $DATA_5$' and outputs a phase-adjusting signal to the phase-controllable frequency divider 880 according to the initial position difference d_{ini}. Next, the phase-controllable frequency divider 860 adjusts the phase of an outputted frequency-divided signal. In this embodiment, because the reproduced EFM signal is not available after the recording operation starts, the phase-shift detector 870 detects the initial position difference d_{ini} of the recorded data block $DATA_5$' and memorizes ~~itbefore~~ it before the recording operation starts. After the recording operation starts, the phase-shift detector 870 outputs a phase-adjusting signal to the phase-controllable frequency divider 880 according to the memorized initial position difference d_{ini}, so that the data lengths of following data blocks are gradually reduced. In the end, the end position of the data block $DATA_8$' is aligned to a correct position.

In paragraph [0049]:

Concerning a data block $DATA_5$" having been recorded onto the recordable optical disk ~~at~~ during a previous recording operation and having a data length shorter than a desired data length defined by the data block ~~$DATA_5$. When~~ $DATA_5$, when the logical address detector 900 receives the reproduced EFM signal generated from the data block $DATA_5$" recorded on the recordable disk, the logical address detector 900 detects a logical address of the data block $DATA_5$". In addition, the physical address is detected by the physical address detector 890 through a well-known push-pull signal read from the recordable optical disk. Then, the position difference detector 880 detects an initial position difference D_{ini} of the recorded data block $DATA_5$" and memorizes ~~itbefore~~ it before the recording operation starts. After the recording operation starts, the position

difference detector 880 outputs a phase-adjusting signal to the phase-controllable frequency divider 880 according to the memorized initial position difference D_{ini}, so that the data lengths of following data blocks are gradually increased. In the end, the end position of the data block $DATA_8$" is aligned to a precise position.

In paragraph [0050]:

Please refer to Fig.17, which is a block diagram of another system 910 according to the present invention. The system 910 includes a recorder 990, a phase-shift detector 970, a phase detector (PD) 920, a charge pump 930, a loop filter 940, a voltage-controlled oscillator (VCO) ~~950,and~~ 950, and a frequency divider 960. The function of the PD 920, the charge pump 930, the loop filter 940, the VCO 950, and a frequency divider 960 is the same as that of the those components of the same name in the related art PLL 10, and the ~~functionof~~ function of the phase-shift detector 970 is the same as that of the PLL system 110, so that the lengthy description is omitted here for simplicity. The recorder 990 receives the output clock from the VCO 950 as the reference clock for recording data, and further receives the phase-adjusting signal from the phase-shift detector 970 for inserting or deleting one bit or more of recording data to be recorded. Please refer to Fig.18 that is a timing diagram illustrating the operations of the recorder 990 in the application of DVD+R/RW or DVD-RW, where a normal frame of recording data contain 1488 recording bits. As shown in Fig. 18(a), if the phase-shift detector 970 is disabled, the length of the frame 1, frame 2, and frame 3 is normal and equal to 1488T. As shown in Fig. 18(b), when the phase-shift detector 970 detects that the phase of the output lock lags the ideal phase, the recorder 990 deletes the last bit of the frame 1' and the deleted bit is discarded to be recorded, which leads the position of the following frame 2' and frame 3'. As shown in Fig. 18(c), when the phase-shift detector 970 detects that the phase of the output lock leads the ideal phase, the recorder 990 inserts one dummy bit at the end of the frame ~~1"and~~ 1" and the inserted dummy bit is recorded, which lags the position of the

following frame 2" and frame 3". By deleting or inserting one bit at the end of a frame according to the phase-adjusting signal, the recorder 990 can compensate the phase shift detected by the phase-shift detector 970.

In paragraph [0051]:

In contrast to the related art, the present invention provides a phase-controllable frequency divider positioned at the feedback path. Therefore, the problem of related art phase shift phenomenon is solved through tuning the phase-controllable frequency divider, and the recording quality is greatly improved. Besides, no matter how ~~largethe~~ large the phase shift is, the claimed invention is capable of making the phase of an output clock locked to a correct ~~phase.In~~ phase. In addition to a reference of the recording data, the output clock can also be a reference for controlling the rotation of the recordable optical disk in a CLV (Constant-Linear Velocity) speed.